Remarks:

The foregoing amendments and these remarks are responsive to the final Office action dated November 10, 2005.

Prior to entry of this Amendment, claims 2-9, 17-20, 22-25, 27-30 and 36-40 remained pending in the application. All claims stand rejected under 35 U.S.C. §103(a) based on Kasamoto et al. (US 6,056,391) in view of Feinn et al. (US 6,260,952). Applicants respectfully disagree.

Nevertheless, in the interest of furthering prosecution on the merits, applicants have cancelled claims 22-25 and 27-30, without prejudice. No claims have been added. None have been amended or withdrawn. Claims 2-9, 17-20, and 36-40 thus remain pending in the present application.

Applicants respectfully request reconsideration of the application and allowance of the pending claims. In the event that the Examiner does not determine that the present application is hereby placed in allowable form, the Examiner is asked to nonetheless enter the present amendments so as to clarify the outstanding issues for appeal.

Declaration Under §1.130

In the November 10, 2005 Office action, the Examiner indicates that Feinn et al. "is available as a reference under 35 U.S.C. § 102(a) and also available as a reference under 35 U.S.C. § 103(a)," and thus rejects applicants' claims based on Kasamoto et al. in view of Feinn et al. under 35 U.S.C. § 103(a).

Applicants, however, assert that Feinn et al. is not available as prior art, and thus, that the rejection under 35 U.S.C. § 103(a) must be withdrawn. In support, applicants provide herewith a Declaration Under § 1.130, demonstrating: (1) that the

present application and Feinn et al. are currently owned by the same party, and (2) that applicants are prior inventors of the subject matter.

Pursuant to 37 C.F.R. § 1.130(a), when any claim of an application is rejected under 35 U.S.C. §103 on a U.S. patent which is not prior art under 35 U.S.C. §102(b), the applicant may disqualify the patent as prior by submitting: (1) a terminal disclaimer; and (2) a declaration stating that the application and patent are currently owned by the same party, and that the inventor(s) named in the application is/are the prior inventor(s). See also, MPEP 718.

Feinn et al. is cited by the Examiner as disclosing "an ink jet printhead having a plurality of resistors for causing ink ejection when applied by an electrical power, wherein each of the resistors is connected to a power/control source through two traces, wherein the traces are dropped through similar-in-structure vias." Applicants respectfully disagree with this characterization of Feinn et al.

Additionally, even if Feinn et al. did disclose such an ink jet printhead, applicants assert that they are prior inventors of the indicated subject matter (that their invention was prior to April 22, 1999). Applicants also assert that both the present application and Feinn et al. are owned by the same party, namely Hewlett-Packard Development Company L.P. These assertions are made by all of the inventors listed in the present application in the presently-provided Declaration Under § 1.130. Applicants also now provide a terminal disclaimer in accordance with § 1.321(c).

Accordingly, pursuant to 37 C.F.R. § 1.130(a), Feinn et al. is disqualified as prior art, and the rejection of claims 2-9, 17-20, and 36-40 under 35 U.S.C. § 103(a) should be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

As noted above, claims 2-9, 17-20, 22-25, 27-30 and 36-40 stand rejected under 35 U.S.C. § 103(a) based on Kasamoto et al. in view of Feinn et al. Although applicants respectfully disagree with the Examiner's characterization of the cited references, claims 22-25 and 27-30 have been cancelled without prejudice. Claims 2-9, 17-20 and 36-40 thus remain pending, after entry of the above amendments.

Kasamoto et al. discloses a substrate with a layered electrode structure for use in an ink jet head. According to the Examiner (applicant disagrees), the layered electrode structure of Kasamoto et al. as having a power via (1105) with a separation barrier. However, the Examiner acknowledges that Kasamoto et al. "does not disclose a controller via that is in the same structure with the power via and connects the at least one resistor to a controller//FET bus."

In fact, the arrangement depicted in Kasamoto et al. would make any form of dual via structure inoperable. As depicted in Fig. 1A of Kasamoto et al., through-holes (1105) connect heat generating portion (1102) to an upper electrode layer (1110c) that spans the device. Providing through-holes on the opposite sides of heat generating portions (1102) would short the heat generating portions, and render them inoperable.

Furthermore, Kasamoto et al. would not perceive any need for a dual via structure because conventional structure would place the either the power bus or the control bus in the same plane as electrode layer (1110a). One side of each heat generating portion thus would have a direct connection to the power/control bus. Such structure is, in fact, shown in Fig. 1A of Kasamoto et al. The indicated via structure (1105) thus would only have utility only on the one side of heat generating

portion (1102) so as to connect connection electrode layer (1110d) to upper electrode layer (1110c).

Nevertheless, the Examiner assumes that via structure may be employed on both sides of heat generating portion (1102), and cites Feinn et al. as suggesting use of similar via structure to connect to power and control sources. Applicants respectfully disagree, noting that the proposed combination would render Kasamoto et al. inoperable, and that Feinn et al. does not disclose opposite power and control vias of a resistor as the Examiner proposes.

Feinn et al. discloses apparatus for routing power and ground lines in an ink-jet printhead. Routing structure includes vias (153, 155 and 157) which are expressly "not covered by the ink barrier layer 112." Feinn et al. thus expressly teaches against use of vias with an ink barrier layer, as the Examiner asserts is taught by Kasamoto et al.

Furthermore, contrary to the Examiner's assertion, Feinn et al. fails to disclose or suggest power and control vias connecting a resistor to power and control busses, respectively. Applicants refer, for clarity, to Fig. 5 of the present application (a portion of which is reproduced below):

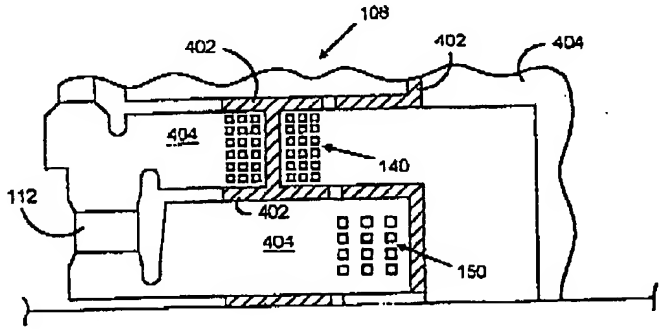

FIG. 5

As will be appreciated from careful review of the above illustration, resistor 112 is connected to power through power vias 140, and is connected to a control signal through FET vias 150. Power vias 140, it will be appreciated, drop from second metal layer 404 to first metal layer 402 in a first array of power vias (to the left if Fig. 5), and then rise back up to the first metal layer in a second array of power vias (to the right in Fig. 5). The power vias thus are employed despite the presence of the both the resistor and power bus (and their respective electrical connection portions) in the same plane (second metal layer 404).

The power/FET vias each employ a separation barrier to create separation between the power/control buses and ink contamination that may occur upon resistor fracture. Resistor 112 thus is fully isolated from the power/control busses by the separation barriers. This is despite the presence of the resistor in a common plane with the power bus.

Neither Kasamoto et al., nor Feinn et al., nor any combination thereof, disclose or suggest both power and control vias formed within a circuit as an interface between a first metal layer and a second metal layer, wherein, at the vias, the second metal layer comprises a separation barrier located adjacent the first metal layer and between at least one resistor of the plural resistors and the power/controller bus, as recited in applicants claims. Furthermore, neither Kasamoto et al., nor Feinn et al., indicate any need for such structure as neither considers introducing a via and return via along a electrical connection path so as to establish an ink barrier. Kasamoto et al. actually teaches directly contrary to the proposed structure. Feinn et al. teaches nothing more than that vias (153, 155 and 157) by which "power lines" (142 and 144) and "gold lines" (143) are electrically

coupled to their respective bond pads may be "similar in structure and function to the via 155." There is no discussion of any use of similar-in-structure vias on opposite sides of a resistor, as the Examiner contends.

For at least the foregoing reasons, the rejection of claims 2-9, 17-20 and 36-40 under 35 U.S.C. § 103(a) based on Kasamoto et al. in view of Feinn et al. should be withdrawn.

Conclusion

Applicants believe that this application is now in condition for allowance, in view of the above amendments and remarks. Accordingly, applicants respectfully request that the Examiner issue a Notice of Allowability covering the pending claims. If the Examiner has any questions, or if a telephone interview would in any way advance prosecution of the application, please contact the undersigned attorney of record.

Respectfully submitted,

KOLISCH HARTWELL, P.C.

Walter W. Karnstein
Registration No. 35,565
Customer No. 23581
Portland, Oregon 97204
Telephone: (503) 224-6655
Facsimile: (503) 295-6679
Attorney for Applicants

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to Examiner L. Nguyen, Group Art Unit 2853, Assistant Commissioner for Patents, at facsimile number (571) 273-8300 on February 8, 2006.

Christie A. Doolittle